

IN THE CLAIMS:

1. -17. (Canceled)

18. (Original) A method for synchronization of at least two clocks connected to a downhole network comprising: a controlling processing element comprising a synchronizing clock sending a first request to a downhole processing element comprising at least one downhole clock to set the downhole clock to time  $t_{sub.n}$ ; the controlling processing element sending a second request to the downhole processing element to relay a time  $t_{sub.z}$  back to the controlling processing element, time  $t_{sub.z}$  being the time according to the downhole clock at the approximate instant the second request is received; the controlling processing element receiving time  $t_{sub.z}$  from the downhole processing element and recording a time  $t_{sub.x}$ , time  $t_{sub.x}$  being the approximate instant time  $t_{sub.z}$  arrives from the downhole processing element, according to the synchronizing clock; approximately determining a total signal latency between the controlling processing element and the downhole processing element by logical computations using time  $t_{sub.z}$  and time  $t_{sub.x}$ ; the controlling processing element sending a request to the downhole processing element to set the downhole clock to a synchronizing time adjusted to compensate for total signal latency.

19. (Original) The method of claim 18, wherein the downhole network is housed within a downhole tool string.

20. (Original) The method of claim 19, wherein the downhole network comprises a plurality of downhole components, wherein each downhole component comprises a conductor connecting a communication element in one end and a second communication element in another end.

21. (Original) The method of claim 20, wherein the first and second communication elements are selected from the group consisting of inductive coils, optical fiber couplers, and electrical contacts.

22. (Original) The method of claim 21, wherein the inductive coils are encapsulated in circular, magnetically conductive, electrically insulating troughs.

23. (Original) The method of claim 18, wherein electronic time stamps are used to determine transmission latency between processing elements.

24. (Original) The method of claim 18, wherein at least one of the processing elements comprises hardware that fixes the computational latency to a known constant.

25. (Original) A method for determining total signal latency between at least two processing elements connected to a downhole network comprising: a controlling processing element comprising a first clock sending a first request to a downhole processing element comprising a downhole clock to set the downhole clock to time  $t_{sub.n}$ ; the controlling processing element sending a second request to the downhole processing element to relay a time  $t_{sub.z}$  back to the controlling processing element, time  $t_{sub.z}$  being the time according to the downhole clock at the approximate instant the second request is received; the controlling processing element receiving time  $t_{sub.z}$  from the downhole processing element and recording a time  $t_{sub.x}$ , time  $t_{sub.x}$  being the approximate instant time  $t_{sub.z}$  arrives from the downhole processing element, according to the first clock; the controlling processing element approximately determining a total signal latency between itself and the downhole processing element by logical computations using time  $t_{sub.z}$  and time  $t_{sub.x}$ .

26. (Original) The method of claim 25, wherein the downhole network is housed within a downhole tool string.

27. (Original) The method of claim 26, wherein the downhole network comprises a plurality of downhole components, wherein each downhole component comprises a conductor connecting a first communication element in one end and a second communication element in another end.

28. (Original) The method of claim 27, wherein the first and second communication elements are selected from the group consisting of inductive coils, optical fiber couplers, and electrical contacts.

29. (Original) The method of claim 28, wherein the inductive coils are encapsulated in circular, magnetically conducting, electrically insulating troughs.

30. (Original) The method of claim 25, wherein at least one time  $t_{sub,z}$  and at least one time  $t_{sub,x}$  are measured to determine an approximate average total signal latency between the first and second devices.

31. (Original) The method of claim 25, wherein at least one of the processing elements comprises hardware that fixes the computational latency to a known constant.

32. – 44. (Canceled)

45. (New) The method of claim 25, wherein at least one of the clocks is located outside of the well bore.

46. (New) The method of claim 25, wherein at least one of the downhole clocks is attached to the tool string.

47. (New) The method of claim 25, wherein the downhole clocks are distributed along the tool string.

48. (New) The method of claim 25, wherein the downhole clocks are associated with tools selected from the group consisting of mud motors, turbines, jars, repeaters, amplifiers, nodes, mud hammers, shock absorbers, reamers, under-reamers, fishing tools, steering elements, MWD tools, LWD tools, seismic sources, seismic receivers, sensors, modems, swivels, pumps, perforators, other tools with an explosive charge, mud-pulse sirens, well casing, blow-out preventors, bottom hole assemblies, switches, routers, multiplexers, piezoelectric devices, optical transmitter, optical regenerators, optical receivers, and wireless transceivers.

49. (New) The method of claim 25, wherein at least one of the processing elements is connected to an information source through a medium selected from the group consisting of global positioning systems, computer networks, and wireless networks.

50. (New) The method of claim 25, wherein at least three clocks are concurrently electrically synchronized.

51. (New) The system of claim 25, wherein at least one clock comprises a clock source selected from the group consisting of at least one crystal, at least one transistor, at least one oscillator, at least one RC circuit, at least one LC circuit, and at least one RLC circuit.